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(54) Title of the Invention: DATA TRANSMITTING DEVICE

(54) Abstract

[Problem to be Solved] In a video transmitting device provided with a plurality of microprocessors, to update the programs for all the microprocessors collectively from an external downloading interface.

[Solution] A system control section 1, a video sound encoding section 2, a video sound decoding section 3 and a line control section 4 constituting a video transmitting device have microprocessors 11, 21, 31 and 41 and rewritable nonvolatile memories 13, 23, 33 and 43 for storing a program, respectively. In updating programs, a memory card 6 in which updating programs have been stored is read by a memory card reading section 17 provided in the system control section 1 and the updating programs are stored in the rewritable nonvolatile memories 13, 23, 33 and 43 of the sections via an external downloading interface 14. A collective

update of programs can be thereby realized without causing an increase in the system start-up time at the normal start-up.

[Claims]

[Claim 1] A data transmitting device, comprising: a system control section; a data encoding section; a data decoding section; and a line control section, the system control section having: a rewritable nonvolatile storage means for storing a program for a processor; and an external downloading interface,
the data encoding section, the data decoding section and the line control section each having a rewritable nonvolatile storage means for storing a program,
wherein the programs stored in the rewritable nonvolatile storage means are updated collectively from the external downloading interface of the system control section.

[Claim 2] The data transmitting device according to Claim 1, wherein a storage medium reading section for reading a storage medium is provided in the system control section, wherein the programs for the system control section, the data encoding section, the data decoding section and the line control section are read from the storage medium by the storage medium reading section and the programs stored in the rewritable nonvolatile storage means are updated via the external downloading interface.

[Claim 3] The data transmitting device according to Claim 2, wherein the programs stored in the storage medium have version information, and wherein the system control section recognizes the version information before downloading the programs stored in the storage medium.

[Claim 4] The data transmitting device according to Claim 1, wherein the data encoding section, the data decoding section and the line control section each have a processor, and wherein the processors inform the processor of the system control section of

the version information of the programs stored in the rewritable nonvolatile storage means at start-up of the system and the version information of the programs for the data encoding section, the data decoding section and the line control section is managed collectively in the system control section.

[Claim 5] The data transmitting device according to Claim 4, wherein the processor provided in the system control section compares the versions of updating programs from the external downloading interface with those of the programs stored in the rewritable nonvolatile storage means of the data encoding section, the data decoding section, and the line control section and performs download of programs into processors which need updating.

[Claim 6] The data transmitting device according to Claim 1, wherein the data decoding section has a bus interface which serves as a control data input/output means at the time of downloading a program from the system control section and as a signal incoming data input/output means.

[Claim 7] The data transmitting device according to Claim 1, wherein the line control section has a bus interface which serves as a control data input/output means at the time of downloading a program from the system control section and as a signal outgoing data input/output means.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a data transmitting device provided with a plurality of processors such as a video transmitting device, and, more particularly, to a data transmitting device in which programs for a plurality of processors can be collectively updated from outside.

[0002]

[Related Art]

Conventionally, when there arises a need to change a program in a video transmitting device provided with a plurality of microprocessors, the program is updated by replacing a nonvolatile memory, such as a ROM, in which the program is stored. However, in video transmitting devices, which are often used in a rack mount configuration, this method causes a problem that a lot of time and a large number of man-hours are required and a risk of inconsistency of versions due to human error in replacing a plurality of nonvolatile memories.

[0003]

To solve the problems, a device of the type which is provided with a rewritable nonvolatile memory and an external downloading interface so that program update can be made with a memory card or through serial communication has been proposed. In general, however, not all the programs for the microprocessors are updated and, in many cases, update of the program for a system control section with a high possibility of program update from outside is allowed. In reality, however, there are many cases in which the programs for every section, in addition to the program for the system control section, have to be changed simultaneously according to the type of the line interface or customization, and it is desired to perform program update in all the microprocessors in the device collectively from outside in view of maintainability.

[0004]

As a method for performing program update in all the microprocessors in a device from outside, a method shown in FIG. 6 has been proposed. In this drawing, programs for all the processors are stored in a rewritable nonvolatile memory 73 provided in a master processor section 7, and program update in all the processors can be performed from the external downloading interface 74. Only a volatile memory 82 is provided in a slave processor

section 8, and a program necessary at the start-up is downloaded from the master processor section 7 to the volatile memory 82 of the slave processor section 8 (see JP-A-Hei 7-36704).

[0005]

[Problem to be Solved by the Invention]

In the conventional program update method shown in FIG. 6, since only the master processor section 7 has the rewritable nonvolatile memory 73 for storing programs, programs corresponding in number to the microprocessors of the slave processor must be downloaded at the start of the system. Therefore, there is a problem that the more the number of the microprocessors is, the longer the start-up time is.

[0006]

The present invention has been made to solve the above problem. It is, therefore, an object of the present invention to provide a data transmitting device in which program update in all the processors in the device can be performed collectively from an external downloading interface without causing an increase in the system start-up time with an increase in the number of microprocessors. Another object of the present invention is to provide a data transmitting device with high maintainability in which the programs for all the microprocessors are stored in one memory card to avoid the risk of inconsistency of program versions in every section.

[0007]

[Means for Solving the Problem]

For the purpose of accomplishing the above objects, the present invention has a system control section; a data encoding section; a data decoding section; and a line control section, the system control section having: a rewritable nonvolatile storage means for storing a program for a processor; and an external downloading interface, the data encoding section, the data decoding section

and the line control section each having a rewritable nonvolatile storage means for storing a program, and the programs stored in the rewritable nonvolatile storage means are updated collectively from the external downloading interface of the system control section. By this configuration, since the microprocessor in each section executes the program stored in a dedicated rewritable nonvolatile storage means when there is no need for program update, there is no need for the download process from the master processor to the slave processor which is performed every time the system is started in a conventional system and the system can be started quickly.

[0008]

Also, a storage medium reading section for reading a storage medium is provided, and the programs for the system control section, the data encoding section, the data decoding section and the line control section are read from the storage medium by the storage medium reading section and the programs stored in the rewritable nonvolatile storage means are updated via the external downloading interface. By this configuration, the maintainability at the time when the device is used in a rack mount configuration can be improved.

[0009]

In addition, the programs stored in the storage medium have version information and the system control section recognizes the version information before downloading the programs stored in the storage medium. By this configuration, the system control section can recognize the version information of the programs before downloading the programs.

[0010]

Also, the data encoding section, the data decoding section and the line control section each have a processor. The processors inform the processor of the system control section of the version

information of the programs stored in the rewritable nonvolatile storage means at start-up of the system and the version information of the programs for the data encoding section, the data decoding section and the line control section is managed collectively in the system control section. By this configuration, the version information of the programs for the data encoding section, the data decoding section and the line control section can be managed collectively in the system control section.

[0011]

In addition, the processor provided in the system control section compares the versions of updating programs from the external downloading interface with those of the programs stored in the rewritable nonvolatile storage means of the data encoding section, the data decoding section and the line control section, and performs download of programs into processors which need updating. By this configuration, since download of programs unnecessary to be updated can be skipped, the program download time can be saved and the risk of version downgrading of programs due to human error can be avoided.

[0012]

Also, the data decoding section has a bus interface which serves as a control data input/output means at the time of downloading a program from the system control section and as a signal incoming data input/output means. By this configuration, an increase in size of the device due to addition of a download function can be reduced.

[0013]

In addition, the line control section has a bus interface which serves as a control data input/output means at the time of downloading a program from the system control section and as a signal outgoing data input/output means. By this configuration, an increase in size of the device due to addition of a download function can be reduced.

[0014]

[Embodiment of the Invention]

The invention described in Claim 1 has a system control section; a data encoding section; a data decoding section; and a line control section, the system control section having a rewritable nonvolatile storage means for storing a program for a processor and an external downloading interface, the data encoding section, the data decoding section and the line control section each having a rewritable nonvolatile storage means for storing a program, in which the programs stored in the rewritable nonvolatile storage means are updated collectively from the external downloading interface of the system control section, and has an effect that the programs stored in the rewritable nonvolatile storage means of the sections are updated collectively from the external downloading interface of the system control section.

[0015]

The invention described in Claim 2 of the present invention is the data transmitting device described in Claim 1, in which a storage medium reading section for reading a storage medium is provided in the system control section, wherein the programs for the system control section, the data encoding section, the data decoding section and the line control section are read from the storage medium by the storage medium reading section and the programs stored in the rewritable nonvolatile storage means are updated via the external downloading interface, and has an effect that updating programs for the sections stored in a storage medium are read by the storage medium reading section of the system control section and the programs stored in the rewritable nonvolatile storage means of the sections are updated collectively from the external downloading interface of the system control section.

[0016]

The invention described in Claim 3 of the present invention

is the data transmitting device described in Claim 1, in which the programs stored in the storage medium have version information and the system control section recognizes the version information before downloading the programs stored in the storage medium, and has an effect that the system control section recognizes the version numbers of the programs stored in the storage medium before downloading the programs.

[0017]

The invention described in Claim 4 of the present invention is the data transmitting device described in Claim 1, in which the data encoding section, the data decoding section and the line control section each have a processor, and in which the processors inform the processor of the system control section of the version information of the programs stored in the rewritable nonvolatile storage means at start-up of the system and the version information of the programs for the data encoding section, the data decoding section and the line control section is managed collectively in the system control section, and has an effect that the system control section manages the version information of the programs for the sections collectively.

[0018]

The invention described in Claim 5 of the present invention is the data transmitting device described in Claim 4, in which the processor provided in the system control section compares the versions of updating programs from the external downloading interface with those of the programs stored in the rewritable nonvolatile storage means of the data encoding section, the data decoding section and the line control section, and performs download of programs into processors which need updating, and has an effect that the processor provided in the system control section determines the necessity of update by comparison of the version numbers and performs download of programs into the processors which need

updating.

[0019]

The invention described in Claim 6 of the present invention is the data transmitting device described in Claim 1, in which the data decoding section has a bus interface which serves as a control data input/output means at the time of downloading a program from the system control section and as a signal incoming data input/output means, and has an effect that the bus interface of the data decoding section is used for input and output of control data at the time of downloading a program from the system control section and for input and output of signal incoming data.

[0020]

The invention described in Claim 7 of the present invention is the data transmitting device described in Claim 1, in which the line control section has a bus interface which serves as a control data input/output means at the time of downloading a program from the system control section and as a signal outgoing data input/output means, and has an effect that the bus interface of the line control section is used for input and output of control data at the time of downloading a program from the system control section and for input and output of signal outgoing data.

[0021]

Description is hereinafter made of an embodiment of the present invention with reference to the drawings.

[0022]

As shown in FIG. 1, one example of a video transmitting device to which the present invention is applied has a system control section 1, and a data encoding section 2, a video sound decoding section 3 and a line control section 4 which are connected to the system control section 1 through a system bus 5. Although a system in which video and sound are multiplexed is shown in this example, the present invention is applicable to a system only for video and

a system in which control data such as LSD (Low Speed Data) and HSD (High Speed Data) are multiplexed.

[0023]

The system control section 1 has a microprocessor 11, a volatile memory 12 such as a RAM, a rewritable nonvolatile memory 13 such as a flash EEPROM, an external downloading interface 14, a bus interface 15, and a CPU bus 16 for connecting them. The bus interface 15 is connected to the system bus 5. The external downloading interface 14 is connected to a memory card reading section 17. When a memory card 6 is inserted into the memory card reading section 17, the microprocessor 11 can read information stored in the memory card 6.

[0024]

The video sound encoding section 2 has a microprocessor 21, a volatile memory 22 such as a RAM, a rewritable nonvolatile memory 23 such as a flash EEPROM, a bus interface 25, a multiplexing process section 27, and encoding process section 28, a video sound input section 29, and a CPU bus 26 for connecting them, and a download arbitration means 24. The download arbitration means 24 is connected to the microprocessor 21 and the bus interface 25, and the bus interface 25 is connected to the system bus 5.

[0025]

The video sound decoding section 3 has a microprocessor 31, a volatile memory 32 such as a RAM, a rewritable nonvolatile memory 33 such as a flash EEPROM, a bus interface 35, a separating process section 37, a decoding process section 38, a video sound output section 39, a CPU bus 36 connecting them, and a download arbitration means 34. The download arbitration means 34 is connected to the microprocessor 31 and the bus interface 35, and the bus interface 35 is connected to the system bus 5.

[0026]

The line control section 4 has a microprocessor 41, a volatile

memory 42 such as a RAM, a rewritable nonvolatile memory 43 such as a flash EEPROM, a bus interface 45, a line interface section 47, a CPU bus 46 for connecting them, and a download arbitration means 44. The download arbitration means 44 is connected to the microprocessor 41 and the bus interface 45, and the bus interface 45 is connected to the system bus 5.

[0027]

One example of the structure of data stored in the memory card 6 is shown in FIG. 2. As shown in the drawing, the data stored in the memory card 6 has a region in which programs for the system control section 1, the video sound encoding section 2, the video sound decoding section 3 and the line control section 4 are stored, and a region in which the version numbers of the programs are stored.

[0028]

The program update operation in the video transmitting device constituted as described above is described with reference to the flowchart shown in FIG. 3.

[0029]

When the power of the system is turned on (step S1), the microprocessor 11 of the system control section 1 copies a program stored in the rewritable nonvolatile memory 13 in advance into the volatile memory 12 and executes the program stored in the volatile memory 12 (step S2). The microprocessor 11 first performs a process to determine whether to proceed to a program update process. A determination means is based on information stored in a rewritable nonvolatile memory provided separately from the rewritable nonvolatile memory for storing the program, an instruction by a DIP switch, or information about whether the memory card 6 has been inserted into the memory card reading section 17 or not. As a result of the determination process, the system proceeds to a program update process or a normal start process (step S3).

[0030]

On the other hand, the microprocessors 21, 31, 41 of the video sound encoding section 2, the video sound decoding section 3 and the line control section 4 respectively copy programs stored in the rewritable nonvolatile memories 23, 33, 43 in advance into the volatile memories 22, 32, 42 and execute the programs stored in the volatile memories when the power is turned on. After informing the microprocessor 11 of the system control section 1 of the versions of the programs which are currently being executed, the microprocessors 21, 31, 41 are shifted to a state for waiting an instruction for transition to a program update process or a normal start process by the download arbitration means 24, 34, 44, respectively.

[0031]

When the system proceeds to the program update process, the microprocessor 11 of the system control section 1 instructs the download arbitration means 24, 34, 44 to shift to the program update process via the bus interface 15, the system bus 5, and the bus interfaces 25, 35, 45 (step S4). The microprocessors 21, 31, 41 of the video sound encoding section 2, the video sound decoding section 3 and the line control section 4 are shifted to the program update process by the download arbitration means 24, 34, 44, respectively, and waits the start of download of updating programs.

[0032]

Then, the microprocessor 11 of the system control section 1 reads the program version information region stored in the memory card 6 connected to the memory card reading section 17 via the external downloading interface 14 and compares the versions of the updating programs stored in the memory card 6 with the version of the program which the microprocessor 11 is currently executing and the versions of the programs which are currently being executed informed from the microprocessors 21, 31, 41 (step S5). The updating programs can be therefore downloaded only into the

processors which need updating (step S6). When the programs for all the processors need forcible updating, this process can be skipped.

[0033]

When the program for the microprocessor 11 of the system control section 1 is updated, a program for the microprocessor 11 from the external downloading interface 14 is expanded in the volatile memory 12 and then written into the rewritable nonvolatile memory 13.

[0034]

When the program for the microprocessor 21 of the video sound encoding section 2 is updated, the microprocessor 11 instructs the download arbitration means 24 to start download via the bus interface 15, the system bus 5 and the bus interface 25. The microprocessor 21 receives a download start instruction from the download arbitration means 24, and returns to a microprocessor 11 a reply to the download start instruction via the download arbitration means 24 and the bus interface 25. When control of, for example, reading or writing of download data and a download end instruction are arbitrated between the microprocessor 11 and the microprocessor 21 in the same manner, a program for the microprocessor 21 from the external downloading interface 14 is expanded in the volatile memory 22 via the bus interface 15, the system bus 5, the bus interface 25 and the CPU bus 26. After the entire program has been expanded in the volatile memory 22, it is written into the rewritable nonvolatile memory 23 (step S7). The programs for the microprocessor 31 of the video sound decoding section 3 and the microprocessor 41 of the line control section 4 are updated following the same procedure (step S8). Therefore, a memory region for storing download programs for the other sections is not necessary in the system control section 1.

[0035]

After the download of programs into the processors which need

updating has been completed (Yes in step S9), the program update determination means is set to a normal start instruction (step S10), and the entire system is restarted (step S11). Then, each microprocessor executes an updating program stored in a non-rewritable nonvolatile memory and the system proceeds to a normal start process (step S12).

[0036]

When the system proceeds to a normal start process, the microprocessor 11 of the system control section 1 instructs the download arbitration means 24 to shift to a normal start process via the bus interface 15, the system bus 5 and the bus interface 25 and then executes an operation program stored in the volatile memory 12. The microprocessors 21, 31, 41 of the video sound encoding section 2, the video sound decoding section 3 and the line control section 4 are shifted to a normal start process by the download arbitration means 24, 34, 44, respectively, and then execute operation programs stored in the volatile memories 22, 32, 42, respectively.

[0037]

An example of the constitution of the bus interfaces 35, 45 of the video sound decoding section 3 and the line control section 4 will be described with reference to FIG. 4 and FIG. 5.

[0038]

The bus interface 35 of the video sound decoding section 3 shown in FIG. 4 has a timing generating section 351 and a FIFO 352 for incoming data and program downloading. The timing generating section 351 is connected to the system bus 5, the CPU bus 36, the download arbitration means 34, and the FIFO352 for incoming data and program downloading. The FIFO 352 for incoming data and program downloading is connected to the system bus 5, the CPU bus 36 and the timing generating section 351. When the video transmitting device is performing a sending/receiving operation, the FIFO 352

for incoming data and program downloading is used as a data FIFO for transmitting video sound multiplex data received through the line from the line control section 4 via the system bus 5 to the separating process section 37 in the video sound decoding section 3. When the FIFO 352 is writable from the system control section 1, it can be used as a data FIFO for transmitting an updating program from an external downloading interface to the volatile memory 32 in updating a program.

[0039]

The bus interface 45 of the line control section 4 shown in FIG. 5 has a timing generating section 451, a FIFO 452 for outgoing data and program downloading and a FIFO 453 for incoming data. The timing generating section 451 is connected to the system bus 5, the CPU bus 46, the download arbitration means 44, the FIFO 452 for outgoing data and program downloading, and the FIFO 453 for incoming data. The FIFO 452 for outgoing data and program downloading and the FIFO 453 for incoming data are both connected to the system bus 5, the CPU bus 36, and the timing generating section 451. When the video transmitting device is performing a sending/receiving operation, the FIFO 452 for outgoing data and program downloading is used as a data FIFO for transmitting video sound multiplex data to be transmitted through the line from the video sound encoding section 2 via the system bus 5 to the line interface section 47 in the line control section 4. When this FIFO 452 is writable from the system control section 1, it can be used as a data FIFO for transmitting an updating program from an external downloading interface to the volatile memory 42 in updating a program.

[0040]

As described above, in the embodiment of the present invention, at the start of the system with no need for program update, no download process occurs between the microprocessors and the system

can be started quickly. Also, since a FIFO is used for transmission of incoming and outgoing data and download of a program in the bus interfaces 35, 45 of the video sound decoding section 3 and the line control section 4, an increase in size of the device can be suppressed even though the device is provided with a program download function.

[0041]

[Effect of the Invention]

As can be understood from the above description, according to the present invention, the system control section, the data encoding section, the data decoding section and the line control section of the data transmitting device each have a rewritable nonvolatile memory for storing a program, and an updating program downloaded from an external downloading interface is stored in the rewritable nonvolatile memory of each section for storing a program. Therefore, there can be obtained the effect that a download process between the microprocessors is not necessary and the system can be started quickly when there is no need for program update.

[0042]

Also, in a data transmitting device often used in a rack mount configuration, the program update in all the microprocessors in the device can be realized with one storage medium. Therefore, there can be obtained the effect that the maintainability can be significantly improved as compared to a conventional method in which a ROM is changed for each circuit board.

[0043]

In addition, there can be obtained the effect that even when the program for the system control section and the program for the line control section must be changed synchronously to comply with a line interface, for example, the risk of version inconsistency can be avoided since all the programs are stored in one storage medium.

[0044]

Also, since the versions of the programs which are currently being executed and the versions of the updating programs are compared at the time of program update, there can be obtained the effect that the risk of updating to old versions of the programs can be avoided.

[0045]

Further, since the control data input/output means for program download serves also as an incoming and outgoing data input/output means in the data decoding section and the line control section, there can be obtained the effect that an increase in the size of the device can be suppressed.

[Brief Description of the Drawings]

FIG. 1 is a block diagram illustrating an example of the constitution of a video transmitting device as an embodiment of the present invention.

FIG. 2 is a view illustrating the structure of data stored in a memory card shown in FIG. 1.

FIG. 3 is a flowchart showing a practical example of a program update process which is executed by a microprocessor of a system control section shown in FIG. 1.

FIG. 4 is a block diagram illustrating an example of the constitution of a bus interface of a video sound decoding section shown in FIG. 1.

FIG. 5 is a block diagram illustrating an example of the constitution of a bus interface of a line control section shown in FIG. 1.

FIG. 6 is a block diagram illustrating a conventional multi-processor system having a program update function.

[Description of Reference Numerals]

1: system control section

2: video sound encoding section

3: video sound decoding section

4: line control section

6: memory card

11, 21, 31, 41: microprocessor

13, 23, 33, 43: rewritable nonvolatile memory

14: external downloading interface

17: memory card reading section

352: FIFO for incoming data and program downloading

452: FIFO for outgoing data and program downloading

FIG. 1

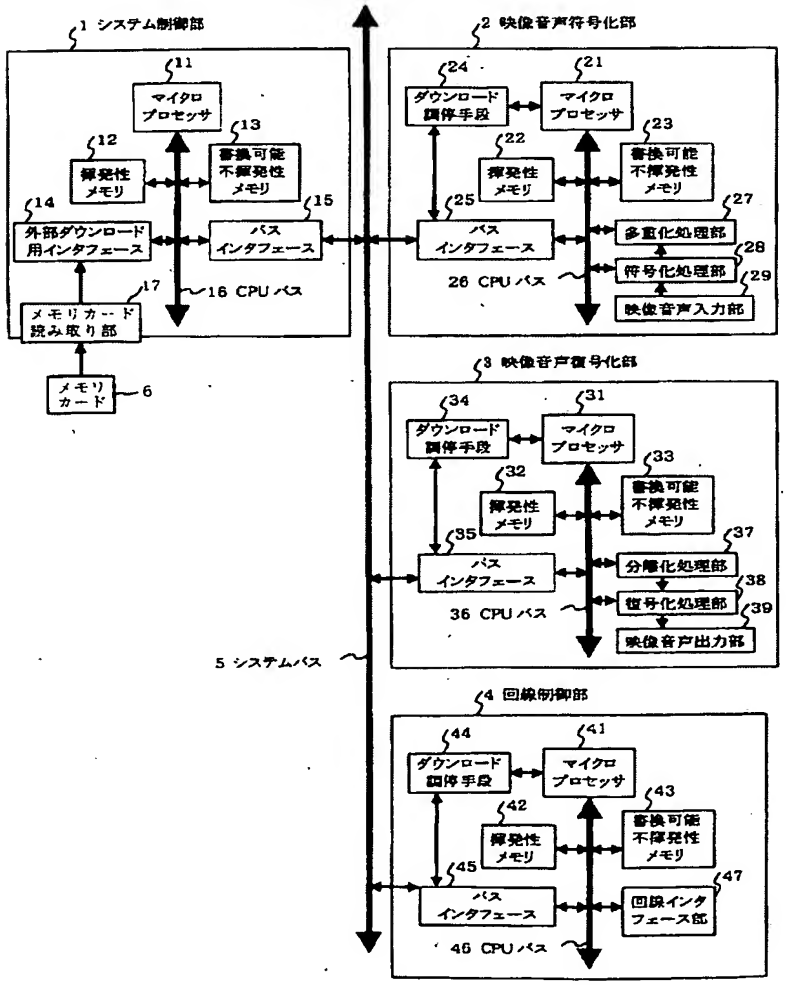

FIG. 1

1: system control section

2: video sound encoding section

3: video sound decoding section

4: line control section

5: system bus

6: memory card

11: microprocessor

12: volatile memory

13: rewritable nonvolatile memory

14: external downloading interface

15: bus interface

16: CPU bus

17: memory card reading section

21: microprocessor

22: volatile memory

23: rewritable nonvolatile memory

24: download arbitration means

25: bus interface

26: CPU bus

27: multiplexing process section

28: encoding process section

29: video sound input section

31: microprocessor

32: volatile memory

33: rewritable nonvolatile memory

34: download arbitration means

35: bus interface

36: CPU bus

37: separating process section

38: encoding process section

39: video sound output section

41: microprocessor

42: volatile memory

43: rewritable nonvolatile memory

44: download arbitration means

45: bus interface

46: CPU bus

47: line interface section

FIG. 2

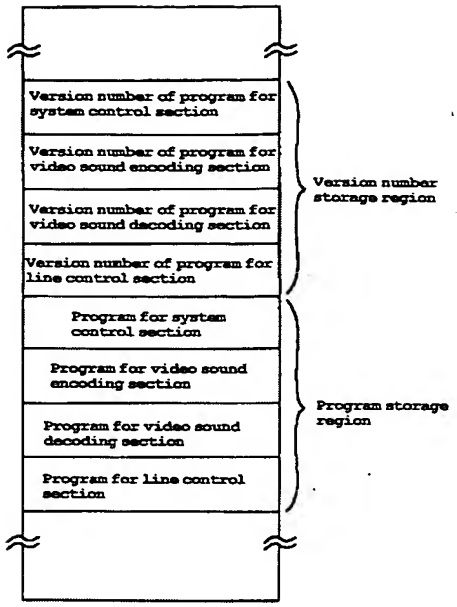

FIG. 3

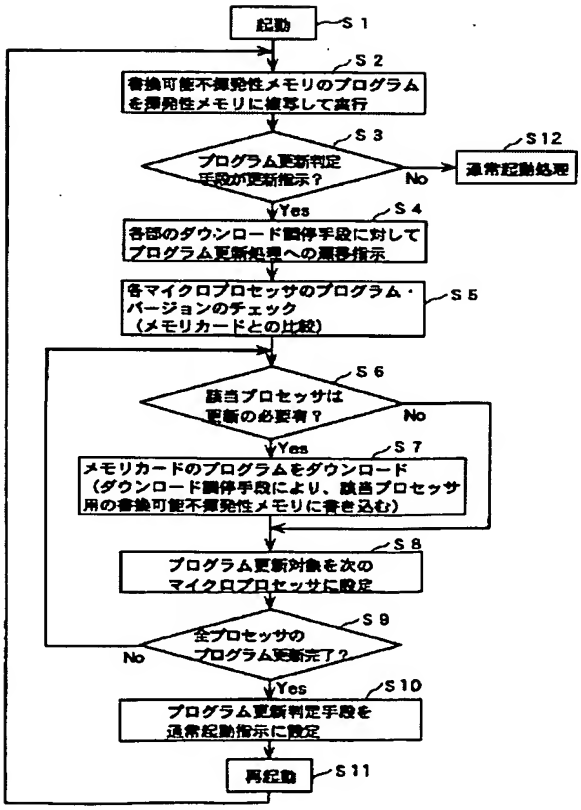

FIG. 3
S1: Start
S2: Copy program, which is stored in rewritable nonvolatile memory, into volatile memory and execute it
S3: Has program update determination means instructed update?
S4: Instruct download arbitration means of every section to shift to program update process
S5: Check program versions of every microprocessor (comparison with memory card)
S6: Does subject processor need updating?
S7: Download program in memory card (written into rewritable nonvolatile memory of subject processor by download arbitration means)
S8: Set next microprocessor as target of program update
S9: Has program update in all processors been completed?
S10: Set program update determination means to normal start instruction
S11: Restart
S12: Normal start process

FIG. 4

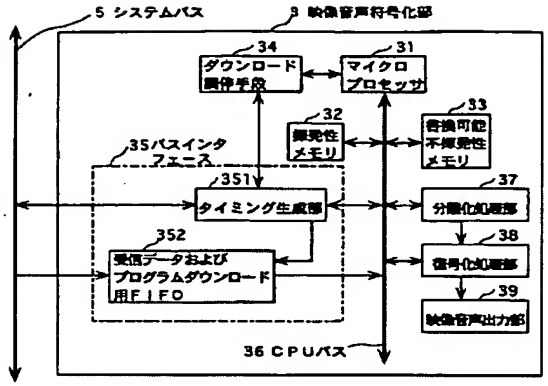

FIG. 4
5: system bus
3: video sound decoding section
31: microprocessor
32: volatile memory
33: rewritable nonvolatile memory
34: download arbitration means
35: bus interface
36: CPU bus
37: separating process section
38: encoding process section
39: video sound output section
351: timing generating section
352: FIFO for program downloading and incoming data

FIG. 5

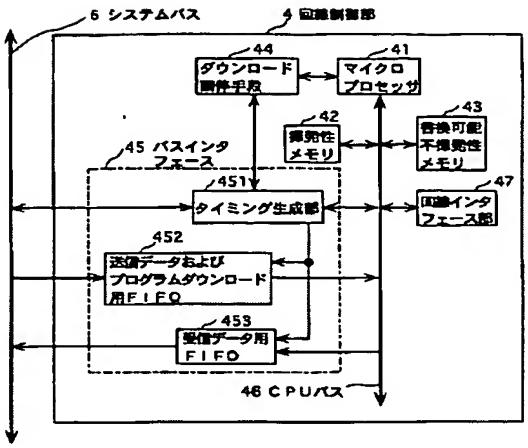

FIG. 5
4: line control section
5: system bus
41: microprocessor
42: volatile memory
43: rewritable nonvolatile memory
44: download arbitration means
45: bus interface
46: CPU bus
47: line interface section
451: timing generating section
452: FIFO for program downloading and outgoing data
453: FIFO for incoming data

FIG. 6

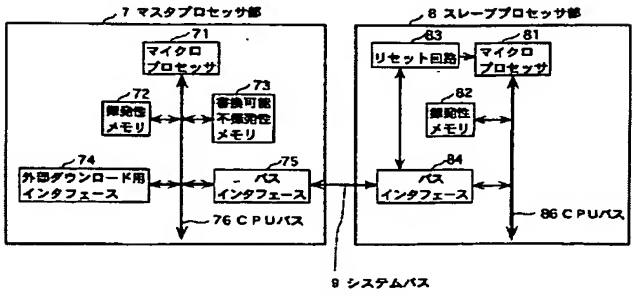

FIG. 6
7: master processor section
8: slave processor section
9: system bus
71: microprocessor
72: volatile memory
73: rewritable nonvolatile memory
74: external downloading interface
75: bus interface
76: CPU bus
81: microprocessor
82: volatile memory
83: reset circuit
84: bus interface
86: CPU bus